Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) An image data reducing device for image data composed of a plurality of components, the image data having data corresponding one-to-one to each pixel with respect to a given component among the plurality of components, and having data common to a plurality of pixels with respect to the other components, the image data reducing device, comprising:

a reduced image data generating circuit ~~receiving~~ that receives image data that is input so that data of each component has a series relationship with each other, and ~~generating~~ that generates image data after being reduced so as to output the image data after being reduced; and

an output control signal generating circuit ~~generating~~ that generates an output control signal ~~for controlling~~that controls whether each component of input image data is output or not based on a decimation pattern of input component that is determined depending on a format of input image data and reduction ratio, ~~wherein~~ the reduced image data generating circuit ~~comprises~~ including a switching circuit ~~controlling the~~that controls a presence of output for each component of image data input in series based on the output control signal.

2. (Currently Amended) The image data reducing device according to Claim 1, ~~wherein:~~

~~———————~~the output control signal generating circuit ~~comprises~~comprising:

a counting circuit ~~counting~~ that counts input of the given component, and ~~resetting~~ that resets counted value in ~~the~~ a case where the counted value reaches ~~the~~ a

reciprocal number of the reduction ratio so as to restart counting, based on information about the format of image data and information about the reduction ratio; and

a decimation pattern information ~~storing~~ that stores unit storing decimation pattern information set in correlation with the counted value of the given component, ~~wherein~~ the output control signal ~~is~~ being generated based on the counted value of the given component and the decimation pattern information.

3. (Currently Amended) An image data reducing device reducing YUV image data, comprising:

a reduced image data generating circuit ~~receiving~~ that receives image data that is input so that data of each component of YUV has a series relationship with each other, and ~~generating~~ that generates YUV image data after being reduced so as to output the YUV image data after reduced; and

an output control signal ~~generating~~ that generates circuit generating an output control signal ~~for controlling~~that controls whether each component of YUV of input image data is output or not based on a decimation pattern of input component that is determined depending on a format of input YUV image data and reduction ratio, ~~wherein:~~

the reduced image data generating circuit ~~comprises~~ including a switching circuit ~~controlling the~~that controls a presence of output for each component of image data input in series based on the output control signal;

the output control signal generating circuit ~~comprises~~including:

a counting circuit ~~counting~~ that counts input of Y component, and ~~resetting~~ that resets counted value in the case where the counted value reaches ~~the~~ a reciprocal number of the reduction ratio so as to restart counting, based on information about the format of image data and information about the reduction ratio; and

a decimation pattern information storing unit ~~storing~~ that stores decimation pattern information set in correlation with the counted value of the Y component; and

the output control signal ~~is~~ being generated based on the counted value of the Y component and the decimation pattern information.

4. (Currently Amended) The image data reducing device according to ~~any of~~ ~~Claims~~Claim 1 ~~through 3, wherein:~~

the reduced image data generating circuit ~~comprises~~ including a common data storing unit ~~retaining~~ that retains the other components or UV component that is input and has data common to a plurality of pixels, the reduced image data generating circuit generating reduced image data by using data stored in the common data storing unit based on the output control signal; and

the output control signal generating circuit ~~determines~~ that determines whether reduced image data is generated by using data stored in the common data storing unit or not, based on the counted value of the Y component and the decimation pattern information, the output control signal generating circuit generating the output control signal directing to generate reduced image data by using data stored in the common data storing unit in ~~the~~ a case where generating of reduced image data by using data stored in the common data storing unit is determined.

5. (Currently Amended) The image data reducing device according to ~~any of~~ ~~Claims~~Claim 1 ~~through 4, wherein:~~

input data ~~is~~ being received as parallel data with bandwidth equal to a bit number of each component; and

the reduced image data generating circuit ~~controls the~~controlling a presence of output for each bit of the parallel data base on the output control signal.

6. (Currently Amended) The image data reducing device according to ~~any of Claims~~Claim 1 ~~through 5~~, ~~wherein:~~

a reduction ratio setting register setting reduction ratio information ~~is~~ being included; and

reduction ratio ~~is~~ being determined based on the reduction ratio information set in the reduction ratio setting register.

7. (Currently Amended) The image data reducing device according to ~~any of Claims~~Claim 1 ~~through 6~~, ~~wherein:~~

a format information setting register setting format information of input image data ~~is~~ being included; and

a format of input image data ~~is~~ being determined based on the format information set in the format information setting register.

8. (Currently Amended) A micro computer comprising the image data reducing device according to ~~any of Claims~~Claim 1 ~~through 7~~.

9. (Currently Amended) An electronic apparatus, comprising:

the micro computer according to Claim ~~7~~8;

an input ~~means for~~ device that inputs data to be processed by the micro computer; and

LCD output ~~means for outputting~~device that displays data that has been processed by the micro computer.